REMARKS

The Office Action dated April 13, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

As a preliminary matter, Applicant appreciates the indication of allowable subject matter in claims 4-7 of the present application. Applicant also appreciates the allowance of claims 9 and 10.

Claims 1, 4 and 11-14 have been amended, and claim 3 has been cancelled without prejudice. New claims 15 and 16 have been added. Applicant submits that the new claims as well as the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-2, 4-8 and 11-16 are pending in the present application and are respectfully submitted for consideration.

Formal Matters

Claim 14 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim has been amended to more clearly recite the subject matter of the present invention, and therefore is responsive to the rejection. Applicant respectfully requests withdrawal of the rejection.

Claims 1, 2, 8 and 11-14 Recite Patentable Subject Matter

Claims 1-3, 8 and 12-14 were rejected under 35 U.S.C. § 102(b) as being anticipated by JP 63-313251 to Mitsubishi Electric Corp. ("Mitsubishi"). Claim 3 has

been canceled without prejudice, and therefore the rejection is now moot. Applicants respectfully traverse the rejection with respect to claims 1, 2, 8 and 12-14.

Claim 1 recites a data input/output (I/O) system connected to an address bus and a data bus comprising a first register that stores data from the data bus in response to an access signal supplied from the address bus, wherein the data is transferred from the first register to a memory as an address signal; and a second register that stores data generated by the memory in response to the data from the first register.

Claim 12 recites a data input/out (I/O) system connected to an address bus and a data bus, comprising a first register that stores data from the data bus in response to an access signal supplied from the address bus; a memory that receives the data stored in the first register and inputs and outputs memory data from and to the data bus using the data as an address signal; and a second register that stores data generated by the memory in response to the data from the first register.

Claim 13 recites a microprocessor comprising a central processing unit (CPU) connected to an address bus and a data bus; a first register that stores data from the data bus in response to an access signal supplied from the address bus; a memory that receives the data from the first register as an address signal to access memory cells therein and inputs and outputs memory data from and to the data bus; and a second register that stores data generated by the memory in response to the data from the first register.

Claim 14 recites a microprocessor connected to a memory comprising a central processing unit (CPU) connected to an address bus and a data bus, in which the central

processing unit generates control data; an address generation circuit that generates a sequence of addresses in response to the control data from the CPU; and a memory control circuit that accesses the memory in accordance with the sequence of addresses from the address generating circuit; and a register that stores data generated by the memory in response to the data from the address generating circuit, wherein the control data indicates start and stop of the address generation circuit.

Applicants respectfully submit that Mitsubishi fails to disclose or suggest at least the features of "a first register that stores data from the data bus in response to an access signal supplied from the address bus ..., and a second register that stores data generated by the memory in response to the data from the first register" recited in claims 1, 12 and 13, and at least the feature of "a register that stores data generated by the memory in response to the data from the address generating circuit, wherein the control data indicates start and stop of the address generation circuit" as recited in claim 14.

The Office Action characterizes Mitsubishi as allegedly disclosing "a first register (6) that stores data from the data bus (4) in response to an access signal supplied from the address bus (3); and a memory (2) that receives the data stored in the first register and inputs and outputs data from and to the data bus using the data as an address signal. ... Mitsubishi also [allegedly] shows a second register (7) connected between the memory and the data bus for storing data from one of the data bus and the memory in response to the access signal."

Applicant respectfully disagrees with the Examiner's characterization of Mitsubishi since it is submitted that Mitsubishi fails to disclose or suggest at least the above-discussed features. In particular, Applicant submits that the address registers H6 and L7 of Mitsubishi are neither comparable nor analogous to the first register and the second register of the present invention. Specifically, the first register of the present invention stores data from the data bus in response to an access signal supplied from the address bus, and the second register of the present invention stores data generated by the memory in response to the data from the first register. Mitsubishi's address registers H6 and L7 do not disclose or teach that which is recited in the claims of the present application.

To qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Mitsubishi does not disclose or suggest each and every feature of pending Claims 1 and 12-14. Accordingly, Applicant respectfully submits that pending Claims 1 and 12-14 is not anticipated by nor rendered obvious by the disclosure of Mitsubishi. Therefore, Applicant respectfully submits that pending Claims 1 and 12-14 are allowable.

As claims 2 and 8 depend from claim 1, Applicant submits that each of these claims incorporates the patentable aspects therein, and therefore are allowable for at least the reasons set forth above with respect to the independent claim, as well as for the additional subject matter recited therein.

Accordingly, Applicant respectfully requests withdrawal of the rejection.

Claim 11 was rejected under 35 U.S.C. § 102(b) as being anticipated by EP 0 554 819 A1 to Matsushita Electric Industrial Co., Ltd. ("Matsushita). Applicant respectfully traverses the rejection.

Claim 11 recites a method for inputting and outputting data comprising, among other steps, the steps of storing data from an address bus in a first register in response to an access signal supplied from the address bus; and storing data generated by the memory in a second register in response to the data from the first register. Applicant respectfully submits Matsushita does not teach or suggest at least such steps.

As characterized by the Office Action, Matsushita allegedly "shows storing an address signal from an address bus in a register; writing data to a storage device in accordance with the address in the register; storing a circulating address signal in the register; and reading data from the storage device in accordance with the circulating address signal stored in the register (throughout col. 2, lines 34-col. 3, line 39)." Put simply, Matsushita fails to disclose or suggest at least the steps of storing data from an address bus in a first register in response to an access signal supplied from the address bus; and storing data generated by the memory in a second register in response to the data from the first register.

To qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Matsushita does not disclose or suggest each and every feature of pending Claim 11. Accordingly, Applicant respectfully submits that pending Claim 11 is not anticipated by

nor rendered obvious by the disclosure of Matsushita. Therefore, Applicant respectfully submits pending Claim 11 is allowable.

Accordingly, Applicant respectfully requests withdrawal of the rejection.

New claims 15 and 16 recites at least the features of "a first register that stores data from the data bus in response to an access signal supplied from the address bus ... ; and a second register that stores data generated by the memory in response to the data from the first register." Applicant submits that the cited prior art fails to disclose or suggest at least such features, and therefore are allowable.

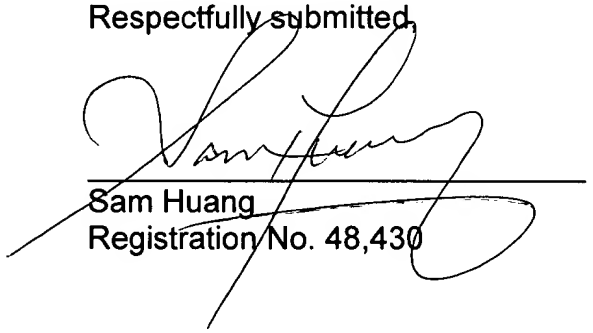
Conclusion

In view of the above, Applicant respectfully submits that each of claims 1, 2, 4-8 and 11-16 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-2, 4-8 and 11-16 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referencing Attorney Docket No. 108075-00017.

Respectfully submitted,



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Enclosures: Petition for Extension of Time (2 months)